ABSTRACT

The present invention relates to a device for generating at least one code phase (C_e, C_p, C_l), the device comprising a shift register (702) comprising N outputs and to which a code sequence (C_{in}) to be phased is applied, and at least one logic branch (722, 723, 724) controlled by at least one combination control signal on the basis of which the logic branch combines the code phase from i outputs of the shift register (702). N is an integer greater than two and i is an integer between 2 and N. Said at least one logic branch preferably comprises i two-input selectors (901 to 909, 911 to 919, 921 to 929), to the first input of each of which is connected one input of the shift register (702) and to the second input is connected one combination control signal (ec0 to ec8, pc0 to pc8, lc0 to lc8), and an i-input combiner (910, 920, 930), to whose outputs are connected the outputs of said i selectors and from whose output said code phase is obtained.

(Figure 9A)